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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/263,766	03/05/1999	TSUYOSHI TOMITA	P8075-9006	2214

7590 10/23/2003

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EXAMINER	
BURD, KEVIN MICHAEL	
ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 10/23/2003

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/263,766	TOMITA, TSUYOSHI	
	Examiner	Art Unit	
	Kevin M Burd	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 July 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

1. This office action, in response to the remarks filed 7/8/2003, is a final office action.

Response to Arguments

2. Applicant's arguments filed 7/8/2003 have been fully considered but they are not persuasive. Applicant states the admitted prior art does not disclose a loop control circuit to monitor the filtered data signal and the feed back signal and controlling the feed back loop based on the monitoring result. However, the control circuit of figure 1 of the instant application's disclosed prior art monitors the data signal, which comprises the filtered signal and the feedback signal. From this data signal, switch 29 is controlled and this switch controls the feedback loop. For this reason, the previous rejections of the claims are maintained and stated below.

3. This examiner mistakenly cited the USC 102(b) section in the previous office action. This has been corrected and the 35 USC 102(a) section is cited below.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

3. Claims 1-4, 6-12, 14 and 15 are rejected under 35 U.S.C. 102(a) as being anticipated by the instant application's disclosed prior art.

Regarding claims 1, 9 and 15, the instant application's disclosed prior art, specifically figure 1, discloses a signal processing circuit. Element 12 is the decision feedback equalizer (page 1, lines 10-15). The equalizer waveform equalizes a digital signal (RD) in accordance with a clock signal (CLK).

A timing recovery phase locked loop (element 16) is disclosed for generating a clock signal. The clock signal will have substantially the same phase as the digital signal once equalization has been achieved. Element 12 comprises a prefilter 21, a decision circuit connected to the prefilter 22, a shift register 24 connected to the decision circuit, a feedback filter 25 and a loop control circuit 17 which monitors the output data signal and controls the switches.

Regarding claim 2, the disclosed prior art of figure 1 discloses the loop control circuit 17, controls the feedback loop by controlling switch 29.

Regarding claims 3 and 10, the disclosed prior art controls one of the inputs to the decision circuit 22. The decision circuit calculates an error between the filtered signal and the feedback signal. This signal affects the output data signal, which controls when the switch 29 is open or closed.

Regarding claims 4 and 12, the disclosed prior art discloses a PLL phase error detection circuit 15, which is connected between the decision circuit and the PLL. The output of the PLL phase error detection circuit is input to the timing recovery PLL.

Regarding claims 6 and 14, the disclosed prior art discloses receiving signals S3, S6 and CLK as shown in figure 1, the detection circuit detects an error between the phase of the read signal and the phase of the clock signal as stated in the last paragraph of page 2. The result of this comparison is output to the PLL.

Regarding claim 7, the signal processor shown in figure 1 includes an adder 22 connected to the prefilter 21 and a comparator 23, which is connected to the adder.

Regarding claims 8 and 11, the comparator will have a predetermined range of useable inputs. The incoming signal must be inside this range for the comparator to function.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 5 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over the instant application's disclosed prior art as applied to claims 1 and 9 above, and further in view of Kobayashi et al (US 5,963,581).

Regarding claims 5 and 13, the instant application's disclosed prior art discloses a signal processing circuit and method for operating the signal processor as stated above. The disclosed prior art does not disclose the detection circuit having a plurality of phase comparison gains. Kobayashi discloses a loop gain switching circuit shown in

figure 3. The circuit of figure 1 receives a signal an outputs the appropriate gain. The gain is controlled by the switches S1 and S2, which allow the gain to be altered.

It would have been obvious for one of ordinary skill in the art at the time of the invention to incorporate the loop gain switching circuit into the signal processor of the disclosed prior art to solve the problem of phase error signals being adversely affected by noise as stated in Kobayashi (column 1, lines 35-54).

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

Any response to this final action should be mailed to:

Box AF
Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314, (for formal communications; please mark "EXPEDITED PROCEDURE" or for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Burd, whose telephone number is (703) 308-7034. The Examiner can normally be reached on Monday-Thursday from 9:00 AM - 6:00 PM.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3800.

Kevin M. Burd
PATENT EXAMINER
10/18/03

MOHAMMAD H. GHAYOUR
PRIMARY EXAMINER